Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

a write circuit which writes a packet that has been received through the link circuit to a randomly accessible packet storage memory; and

a packet division circuit which writes control information of the packet to a control information area of the packet storage memory, writes first data of the packet for a first layer to a first data area of the packet storage memory, and writes second data of the packet for a second layer that is a layer above the first layer to a second data area of the packet storage memory,

wherein the first data is command data used by the serial bus protocol 2 of the first layer and the second data is stream data used by an application layer, and the second data is read sequentially as an uninterrupted stream from the second data area and the read second data is transferred to an application layer device.

2. (Canceled)

3. (Previously Presented) The data transfer control device as defined in claim 1, further comprising:

an area management circuit which makes a full signal go active when the second data area is full, to inhibit the write circuit from writing the second data to the second data area, and makes an empty signal go active when the second data area is empty, to inhibit the second layer from reading the second data from the second data area.

4. (Previously Presented) The data transfer control device as defined in claim 1,

wherein when a request packet which is used for starting a transaction is transmitted to a responding node, transaction identification information comprised within the request packet includes indication information which indicates processing to be performed when a response packet from the responding node is received; and

wherein the control information and the first and second data of the response packet are written into separate data areas as specified by the indication information within the transaction identification information of the response packet, when the response packet from the responding node is received.

5. (Currently Amended) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a circuit which makes transaction identification information within a request packet include indication information which indicates processing to be performed after reception of a response packet from a responding node, when the request packet which is used for starting a transaction is transmitted to the responding node; and

a circuit which performs the processing indicated by the indication information comprised within the transaction identification information of the response packet, wherein control information and data of the response packet are automatically separated and written into at least two of separate hardware, firmware, stream data and command data areas as specified by the indication information within the transaction identification information of the response packet, when the response packet from the responding node is received.

6. (Canceled)

7. (Original) The data transfer control device as defined in claim 5,

wherein a given bit of the transaction identification information is previously reserved as a bit for expressing the indication information.

8. (Original) The data transfer control device as defined in claim 5,

wherein the transaction identification information is a transaction label in accordance with the IEEE 1394 standard.

9. (Currently Amended) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

randomly accessible packet storage memory which stores a packet;

a write circuit which writes a packet that has been received from another node through the link circuit, to the packet storage memory; and

a circuit which reads the packet that has been written to the packet storage memory and transfers the packet to the link circuit;

wherein the packet storage memory is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and the data area is divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer; and

wherein the first data is command data used by the serial bus protocol 2 of the first layer and the second data is stream data used by an application layer, and the second data is read sequentially as an uninterrupted stream from the second data area and the read second data is transferred to an application layer device.

10. (Previously Presented) The data transfer control device as defined in claim 9, further comprising:

a first address storage register which stores a transmission area start address for reserving a transmission area in the second data area;

a second address storage register which stores a transmission area end address for reserving a transmission area in the second data area;

a third address storage register which stores a reception area start address for reserving a reception area in the second data area; and

a fourth address storage register which stores a reception area end address for reserving a reception area in the second data area.

11. (Original) The data transfer control device as defined in claim 10, wherein:

the transmission area start address and the reception area start address are set to the start address of the second data area, and transmission area end address and the reception area end address are set to the end address of the second data area.

12. (Original) The data transfer control device as defined in claim 10, wherein:

both the transmission area start address and the transmission area end address are set to either the start address or the end address of the second data area, the reception area start address is set to the start address of the second data area, and the reception area end address is set to the end address of the second data area.

13. (Original) The data transfer control device as defined in claim 10, wherein:

both the reception area start address and the reception area end address are set to either the start address or the end address of the second data area, the transmission area start address is set to the start address of the second data area, and the transmission area end address is set to the end address of the second data area.

14. (Original) The data transfer control device as defined in claim 1,

wherein data transfer is in accordance with the IEEE 1394 standard.

15. (Original) The data transfer control device as defined in claim 5,

wherein data transfer is in accordance with the IEEE 1394 standard.

16. (Original) The data transfer control device as defined in claim 9,

wherein data transfer is in accordance with the IEEE 1394 standard.

17. (Previously Presented) Electronic equipment comprising:

the data transfer control device as defined in claim 1;

a device which performs given processing on data that has been received from another node through the data transfer control device and a bus; and

a device which outputs or stores data that has been subjected to processing.

18. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 5;

a device which performs given processing on data that has been received from another node through the data transfer control device and a bus; and

a device which outputs or stores data that has been subjected to processing.

19. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 9;

a device which performs given processing on data that has been received from another node through the data transfer control device and a bus; and

a device which outputs or stores data that has been subjected to processing.

20. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 1;

a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus; and

a device which takes in data to be subjected to processing.

21. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 5;

a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus; and

a device which takes in data to be subjected to processing.

22. (Previously Presented) Electronic equipment comprising:

a data transfer control device as defined in claim 9;

a device which performs given processing on data that is to be transferred to another node through the data transfer control device and a bus; and

a device which takes in data to be subjected to processing.

23. (Previously Presented) The data transfer control device as defined in claim 1, further comprising:

a first bus for connecting to an application layer device;

a second bus for controlling the data transfer control device;

a third bus for connecting to a physical layer device;

a fourth bus for connecting to the packet storage memory;

a fifth bus for connecting to a circuit which implements part of the first layer protocol by hardware; and

an arbitration circuit which performs the arbitration for establishing a data path between one of the first, second, third, and fifth buses and the fourth bus.

24. (Previously Presented) The data transfer control device as defined in claim 9, further comprising:

a first bus for connecting to an application layer device;

a second bus for controlling the data transfer control device;

a third bus for connecting to a physical layer device;

a fourth bus for connecting to the packet storage memory;

a fifth bus for connecting to a circuit which implements part of the first layer protocol by hardware; and

an arbitration circuit which performs the arbitration for establishing a data path between one of the first, second, third, and fifth buses and the fourth bus.

25. (Previously Presented) The data transfer control device as defined in claim 1,

wherein the link circuit comprises a tag generation circuit which generates a tag being information for delimiting writing areas;

wherein the packet division circuit writes control information of the packet to the control information area, writes the first data of the packet for the first layer to the first data area, and writes the second data of the packet for the second layer to the second data area, based on a tag generated by the tag generation circuit.

26. (Previously Presented) The data transfer control device as defined in claim 1,

wherein the first data area is an operational request block area and the second area is a stream area.

27. (Previously Presented) The data transfer control device as defined in claim 9,

wherein the first data area is an operational request block area and the second area is a stream area.

28. (Previously Presented) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

randomly accessible packet storage memory which stores a packet;

a write circuit which writes a packet that has been received from another node through the link circuit, to the packet storage memory; and

a circuit which reads the packet that has been written to the packet storage memory and transfers the packet to the link circuit;

wherein the packet storage memory is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and the data area is divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer, and the packet storage memory further comprises:

a first address storage register which stores a transmission area start address for reserving a transmission area in the second data area;

a second address storage register which stores a transmission area end address for reserving a transmission area in the second data area;

a third address storage register which stores a reception area start address for reserving a reception area in the second data area; and

a fourth address storage register which stores a reception area end address for reserving a reception area in the second data area;

wherein the transmission area start address and the reception area start address are set to the start address of the second data area, and transmission area end address and the reception area end address are set to the end address of the second data area.

29. (Previously Presented) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

randomly accessible packet storage memory which stores a packet;

a write circuit which writes a packet that has been received from another node through the link circuit, to the packet storage memory; and

a circuit which reads the packet that has been written to the packet storage memory and transfers the packet to the link circuit;

wherein the packet storage memory is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and the data area is divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer, and the packet storage memory further comprises:

a first address storage register which stores a transmission area start address for reserving a transmission area in the second data area;

a second address storage register which stores a transmission area end address for reserving a transmission area in the second data area;

a third address storage register which stores a reception area start address for reserving a reception area in the second data area; and

a fourth address storage register which stores a reception area end address for reserving a reception area in the second data area;

wherein both the transmission area start address and the transmission area end address are set to either the start address or the end address of the second data area, the reception area start address is set to the start address of the second data area, and the reception area end address is set to the end address of the second data area.

30. (Previously Presented) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

randomly accessible packet storage memory which stores a packet;

a write circuit which writes a packet that has been received from another node through the link circuit, to the packet storage memory; and

a circuit which reads the packet that has been written to the packet storage memory and transfers the packet to the link circuit;

wherein the packet storage memory is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and the data area is divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer, and the packet storage memory further comprises:

a first address storage register which stores a transmission area start address for reserving a transmission area in the second data area;

a second address storage register which stores a transmission area end address for

reserving a transmission area in the second data area;

a third address storage register which stores a reception area start address for reserving a reception area in the second data area; and

a fourth address storage register which stores a reception area end address for reserving a reception area in the second data area;

wherein both the reception area start address and the reception area end address are set to either the start address or the end address of the second data area, the transmission area start address is set to the start address of the second data area, and the transmission area end address is set to the end address of the second data area.

31. (New) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

a write circuit which writes a packet that has been received through the link circuit to a randomly accessible packet storage memory;

a packet division circuit which writes control information of the packet to a control information area of the packet storage memory, writes first data of the packet for a first layer to a first data area of the packet storage memory, and writes second data of the packet for a second layer that is a layer above the first layer to a second data area of the packet storage memory,

a first bus for connecting to an application layer device;

a second bus for controlling the data transfer control device;

a third bus for connecting to a physical layer device;

a fourth bus for connecting to the packet storage memory;

a fifth bus for connecting to a circuit which implements part of the first layer protocol by hardware; and

an arbitration circuit which performs the arbitration for establishing a data path between one of the first, second, third, and fifth buses and the fourth bus,

wherein the first data is command data used by the protocol of the first layer and the second data is data used by an application layer, and the second data is read sequentially from the second data area and the read second data is transferred to an application layer device.

32. (New) A data transfer control device for transferring data between a plurality of nodes connected to a bus, the data transfer control device comprising:

a link circuit which provides services for packet transfer between nodes;

randomly accessible packet storage memory which stores a packet;

a write circuit which writes a packet that has been received from another node through the link circuit, to the packet storage memory;

a circuit which reads the packet that has been written to the packet storage memory and transfers the packet to the link circuit;

a first bus for connecting to an application layer device;

a second bus for controlling the data transfer control device;

a third bus for connecting to a physical layer device;

a fourth bus for connecting to the packet storage memory;

a fifth bus for connecting to a circuit which implements part of the first layer protocol by hardware; and

an arbitration circuit which performs the arbitration for establishing a data path between one of the first, second, third, and fifth buses and the fourth bus

wherein the packet storage memory is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and the data area is divided into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer, and the first data is command data used by the

protocol of the first layer and the second data is data used by an application layer, and the second data is read sequentially from the second data area and the read second data is transferred to an application layer device.